Beverly Display Solutions

Module No. : BD035KDB03

Revision : Ver 1.0

Customer _____

Approved By	Date	Notes

Rev	Issued Date	Description	Editor
1.0	2012-12-23	Preliminary Specification Release	Vicky Ma

CONTENTS

1. General Description

- 3.5” QVGA, Normally Black, 262K Colors, MVA TFT dot matrix LCD module.
- Viewing Angle: 12 o’clock
- Driving IC: NT39016D
- Logic Voltage : 2.8V(Type)
- Data Interface: 3 Lines SPI and RGB Interface.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 2 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		76.9(W) x 63.9(H) x 3.2(D)	mm
Color TFT 240xRGBx320	Active area	70.08(W) x 52.56(H)	mm
	Display format	320 x RGB x 240	dots
	Color configuration	RGB stripe	-
	Dot pitch	0.219 (RGB) (W) x 0.219(H)	mm
Weight		Approx 29.3	gram

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: RoHS

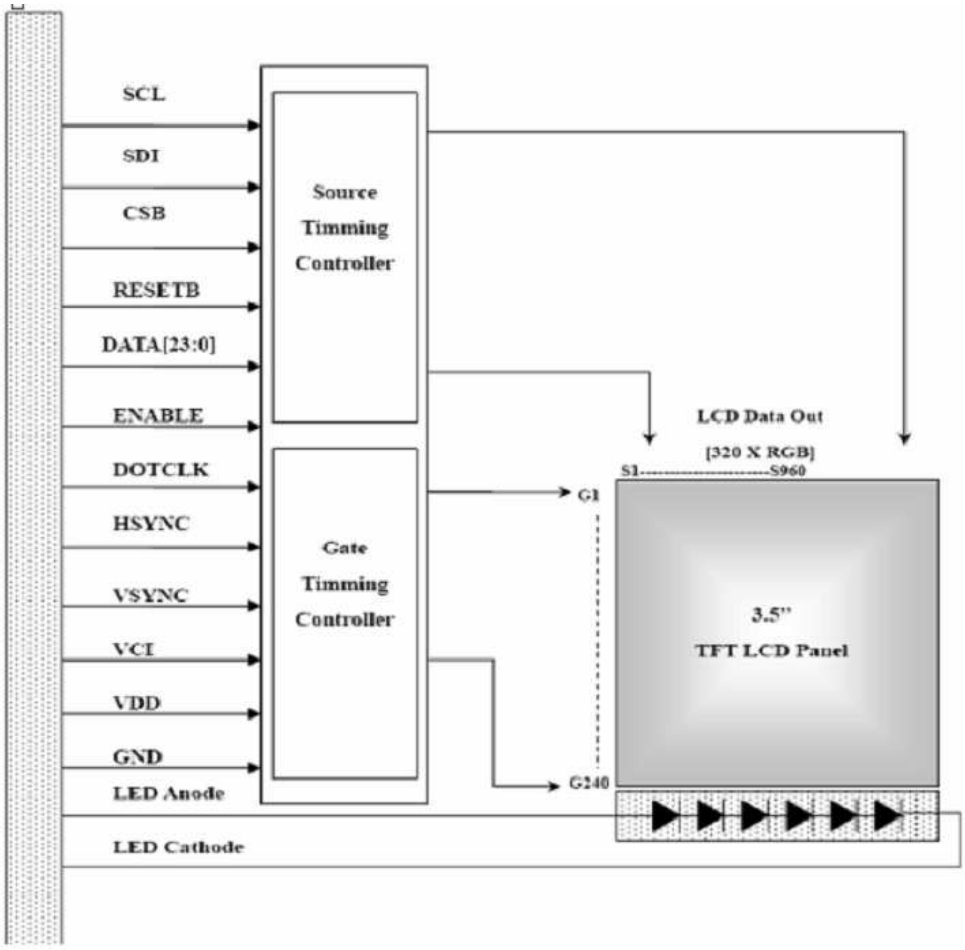


Figure 1: Block Diagram

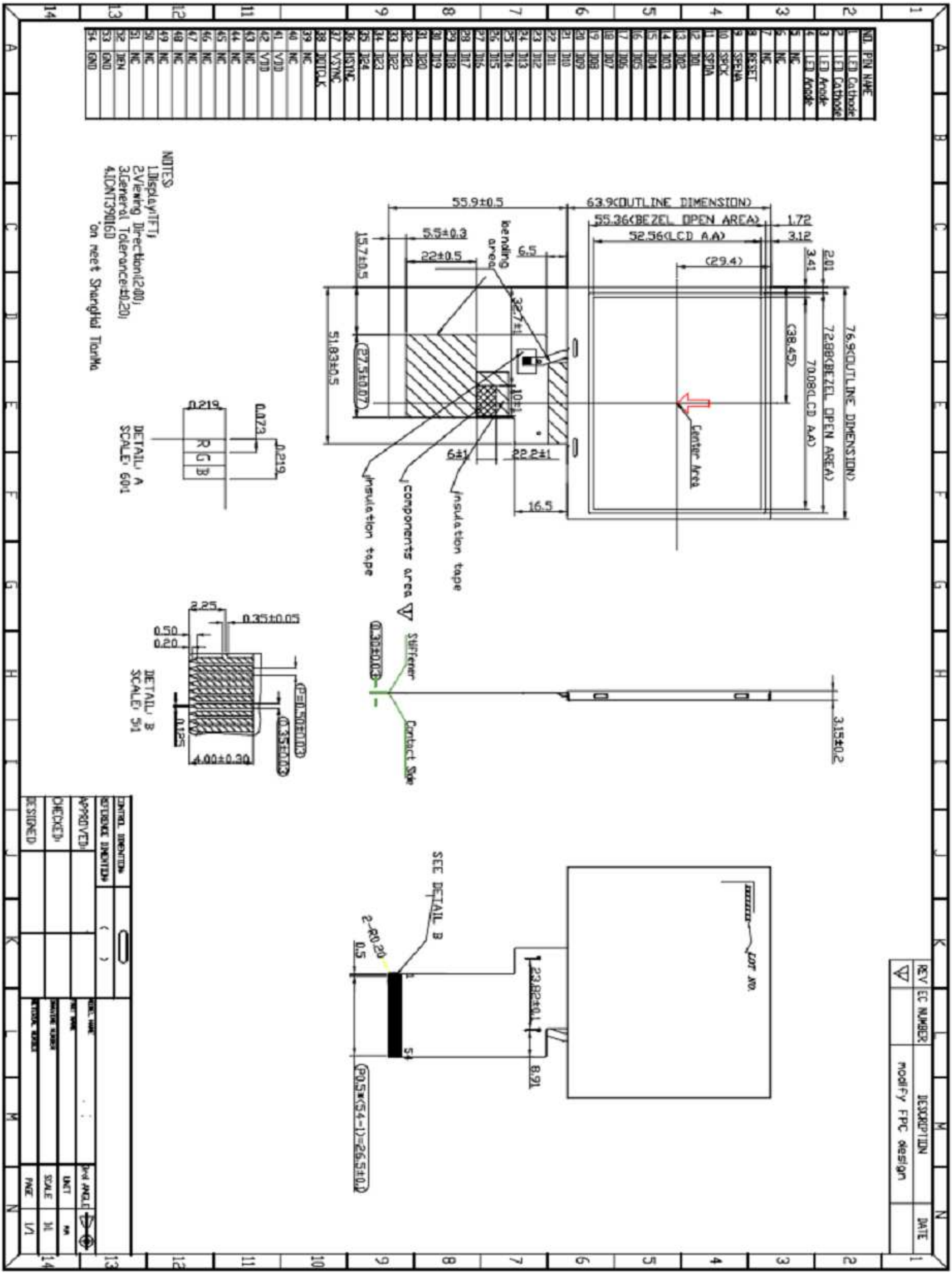


Figure 2: Module Specification

3. Interface Signals

Table 2: Pin assignment

Pin No.	Symbol	Description
1,2	LEDK	Cathode of LED backlight.
3,4	LEDA	Anode of LED backlight.
5,6,7	NC	Dummy pin, Please let it float.
8	RESET	Reset signal. Setting either pin low initializes the LSI. Must be reset after power is supplied.
9	SPENA	Serial port data enable signal
10	SPCK	Serial Clock.
11	SPDA	Serial Data
12~19	B0~B7	Blue Data bus.
20~27	G0~G7	Green Data bus.
28~35	R0~R7	Red Data bus.
36	HSYNC	Horizontal Synchronous Signal
37	VSYNC	Vertical Synchronous Signal
38	DCLK	Dot Data Clock
39,40	NC	Dummy pin, Please let it float.
41,42	VDD	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply.
43~51	NC	Dummy pin, Please let it float.
52	ENB	Data Enable Signal
53,54	GND	Ground.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (VDD)	IOVDD	-0.3	+4.6	V
Power supply voltage (VDD)	VDD	-0.3	+4.6	V
Back Light Forward Current	IF		25	mA
Logic input voltage	VIN	-0.3	IOVDD+0.5	V
Logic output voltage	VOUT	-0.3	IOVDD+0.5	V

Note 1: GND =0V.

Note2: No condensation allowed under any condition.

4.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature(Ta)	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C< 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration(IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half -sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD=2.8.V, GND=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDD		+2.4	+2.8	+3.3	V
Gate drive High voltage	VGH		-	-	-	V
Gate drive Low voltage	VGL		-	-	-	V
Input signal voltage	V_{IH}	"H" level	0.7IOVDD	-	IOVDD	V
	V_{IL}	"L" level	VSSD	-	0.3IOVDD	V
Supply current	ICC+IVDD	IOVDD= +2.8V, Note1	-	6.8	15.0	mA
		VDD = +2.8V, Note 1	-	6.5	15.0	mA
Supply voltage of white LED backlight	VLED	Forward current =20mA(@25°C) Number of LED dies = 5	-	19.2	21.6	V

Note 1: Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. It should change pattern frequently. If the screen is displayed with fixed pattern, use a screen saver.

5.2 Timing Characteristics

5.2.1 Reset Timing Characteristics

At Ta = 25°C, GND=0V, IOVDD=VDD=2.8V.

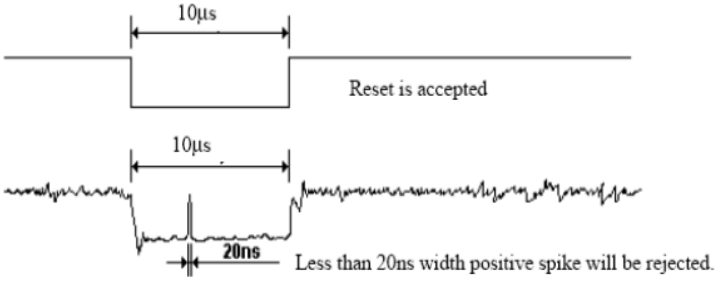
Table 6

Symbol	Parameter	Related Pins	Spec. Min.	Spec. Typ.	Spec. Max.	Note	Unit
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during STB mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

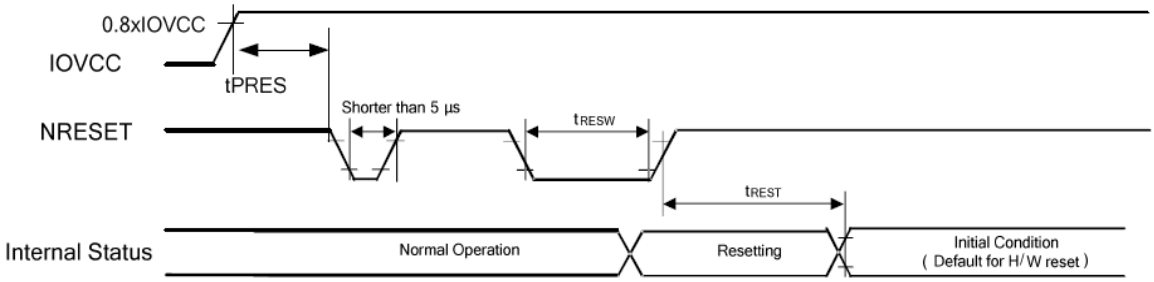


Figure 3: Reset Input Timing

5.2.2 RGB Bus Interface Timing Characteristics

At Ta = 25°C, GND=0V, VDD=2.8V.

Table 7

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Clock Time	Tclk	-	-	35.7	ns	CLK=28MHz
CLK Pulse Duty	Tchw	40	50	60	%	Tclk
HSYNC to CLK	Thc	-	-	1	CLK	
HSYNC Width	Thwh	1	-	-	CLK	
VSYNC Width	Tvwh	1	-	-	Th	
HSYNC Period Time	Th	60.00	63.56	67.00	us	
VSYNC SetupTime	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Set-up Time	Tdsu	12	-	-	ns	D[23:00] to CLK
Data Hold Time	Tdhd	12	-	-	ns	D[23:00] to CLK
DEN Setup Time	Tesd	12	-	-	ns	DEN to CLK

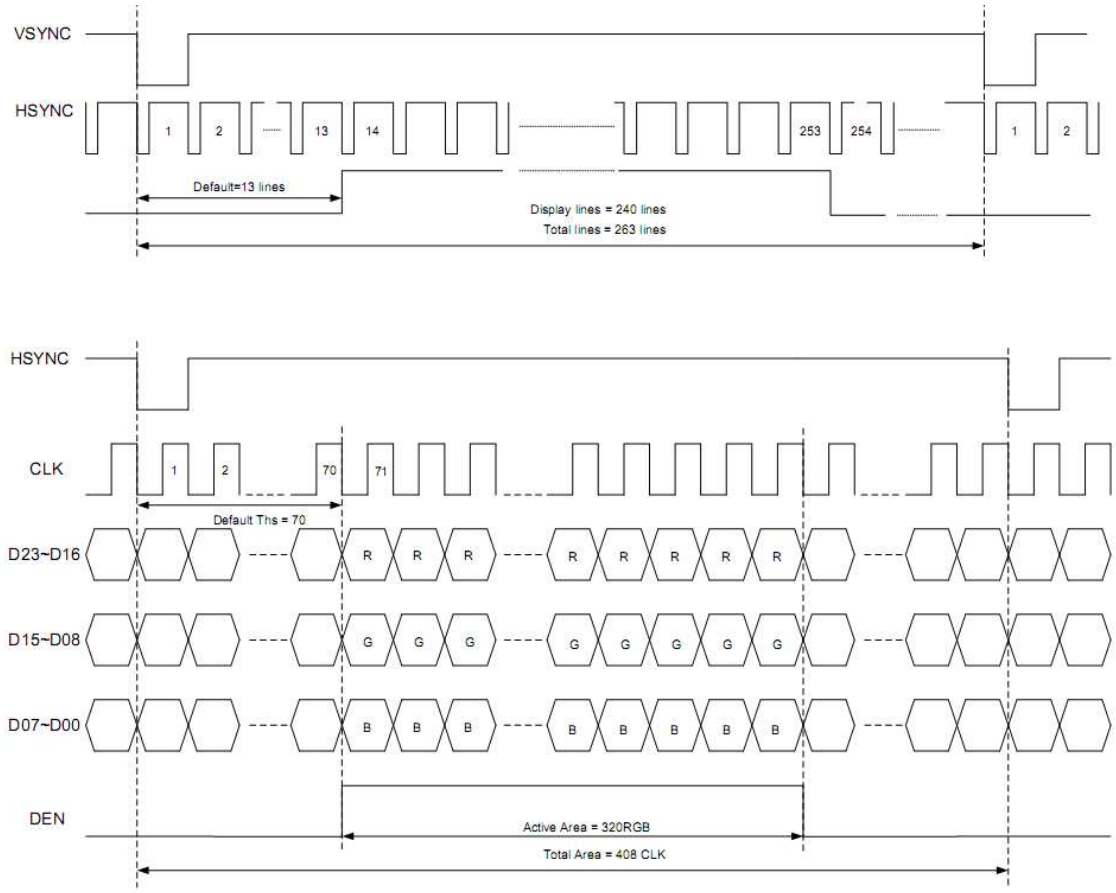


Figure 4: 24 Bit RGB Interface Characteristics

5.2.3 3 lines SPI Interface Timing Characteristics

At Ta = 25°C, GND=0V, VDD=2.8V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Serial Clock	Tspck	320	-	-	ns	
SPCK Pulse Duty	Tscdut	40	50	60	%	
Serial Data Setup Time	Tisu	120	-	-	ns	
Serial Data Hold Time	Tihd	120	-	-	ns	
Serial Clock High/low	Tssw	120	-	-	ns	
Chip Select Distinguish	Tcd	1	-	-	us	

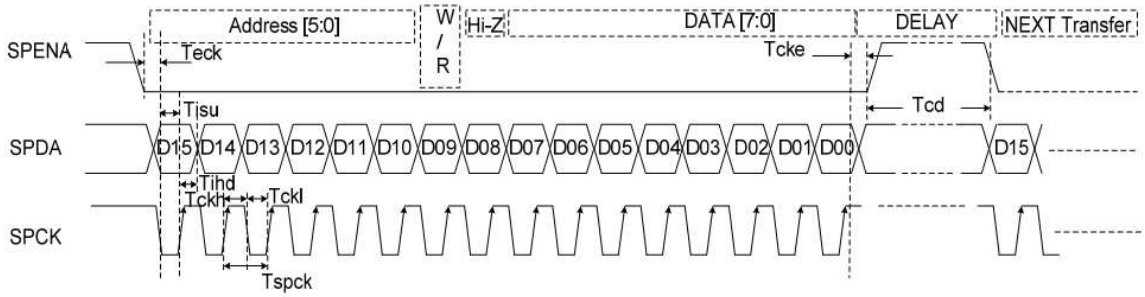


Figure 5: 3 Lines Interface Characteristics

5.2.4 DE Mode Interface Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	24.54/27.00	-	MHz	VDD=3.0~3.6V
CLK cycle time	Tclk	-	40/37	-	ns	
Time that HSYNC to 1'st data input(PAL)	Ths	128	264	-	CLK	
Time that HSYNC to 1'st data input(NTSC)	Ths	128	244	-	CLK	

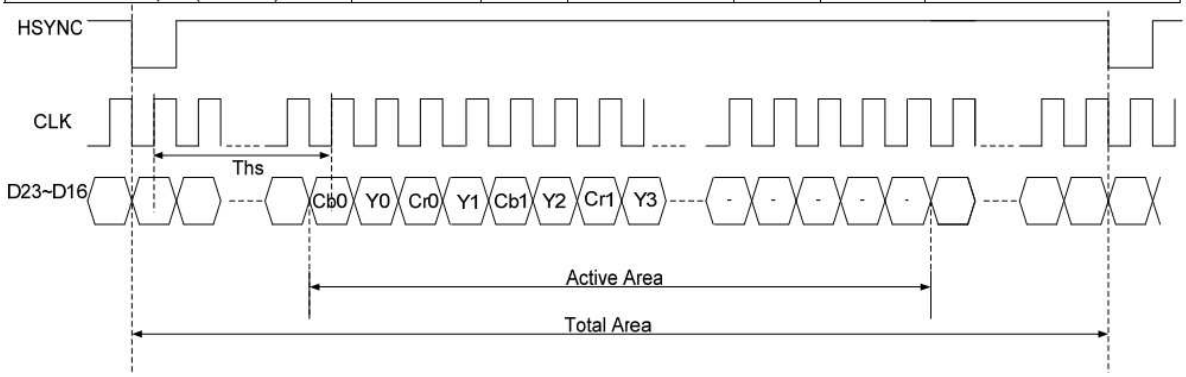


Figure 6: DE Mode Interface Characteristics

5.3 Initial code setting (for reference only)

Table 8(a)

Register	"D/CX"Setting	Data Bus Vaule
Hardware Reset		
Delay 20ms		
Power Supply Setting		
System control register	0	0x00
	1	0x07
Timing Controller function register	0	0x01
	1	0x00
Operation control register	0	0x02
	1	0x03
Input data Format control register	0	0x03
	1	0xCC
Source Timing delay control register	0	0x04
	1	0x46
Gate Timing delay control register	0	0x05
	1	0x0D
Reserved	0	0x06
	1	0x00
Internal function control register	0	0x07
	1	0x00
RGB Contrast control register	0	0x08
	1	0x08
RGB Brightness control register	0	0x09
	1	0x40
Hue / Saturation control register	0	0x0A
	1	0x88
R / B Sub-Contrast control register	0	0x0B
	1	0x88
R Sub-Brightness control register	0	0x0C
	1	0x20
B Sub-Brightness control register	0	0x0D
	1	0x20
VCOMDC Level Control Register	0	0x0E
	1	0x68
VCOMAC Level Control Register	0	0x0F
	1	0xA4
VGAM2 level control register	0	0x10
	1	0x04
VGAM3/4 level control register	0	0x11
	1	0x24
VGAM5/6 level control register	0	0x12
	1	0x24
VCOMDC Trim function control register	0	0x1E
	1	0x00
Wide and narrow display mode control register	0	0x20
	1	0x00

6. Optical Characteristics (for panel only)

Table 9: Optical characteristics

Items		Symbol	Condition		Min.	Typ.	Max.	Unit	Note
Response Time		$T_R + T_F$	Ta=25°C	Viewing normal angle θ=ϕ=0°	-	25	40	ms	(Note 1)
Viewing angle	12’	2	Ta=25°C	Center CR≥10	-	60	-	deg.	(Note 2)
	6’	1			-	40	-		
	9’	2			-	60	-		
	3’	1			-	60	-		
Contrast Ratio		CR	Ta=25°C	Viewing normal angle θ=ϕ=0°	200	350	-	-	(Note 3)
Luminance (on the module surface)		Br	Ta=25°C		140	240	-	cd/m^2	
Transmittance		%			-	3.5	-	%	
Chromaticity	Red	x_R	Ta=25°C	Viewing normal angle θ=ϕ=0°		0.575		-	(Note 4)
		y_R				0.320		-	
	Green	x_G				0.350		-	
		y_G				0.550		-	
	Blue	x_B				0.145		-	
		y_B				0.085		-	
	White	x_W				0.290		-	
		y_W				0.300		-	

Note 1: The electro-optical response time measurements shall be made as Figure 12 by switching the “data” input signal OFF and ON. The times needed for the luminance to change from 10% to 90% s T_r, and 90% to 10% is T_f.

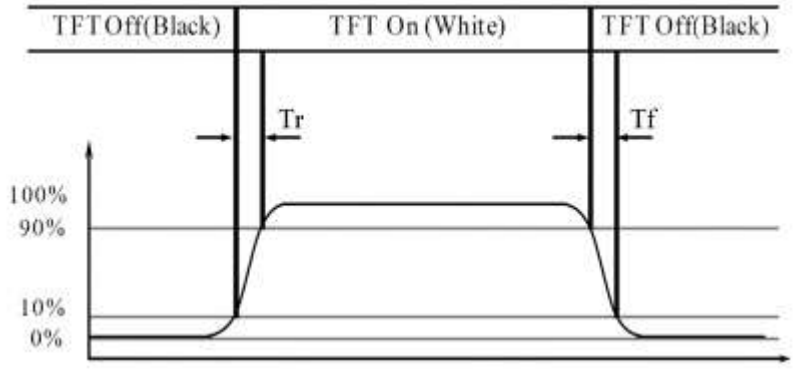


Figure 10: Response Time Testing

Note 2: The definitions of viewing angle.

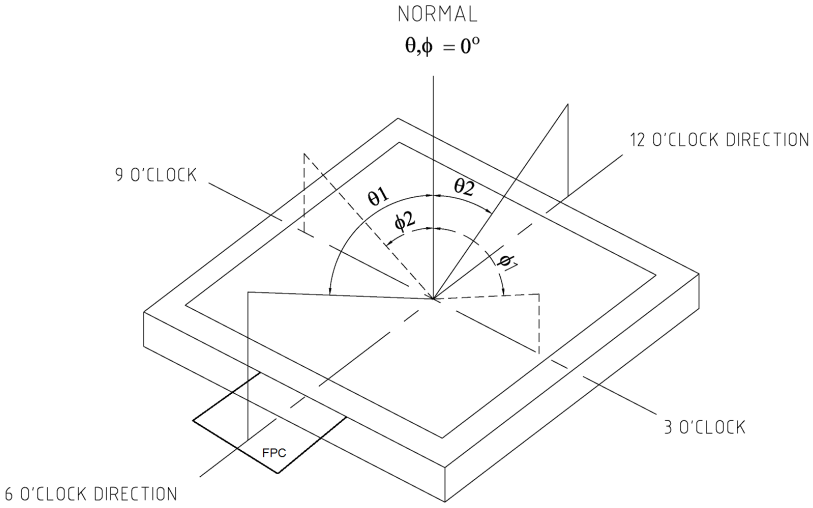


Figure 11

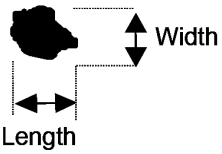
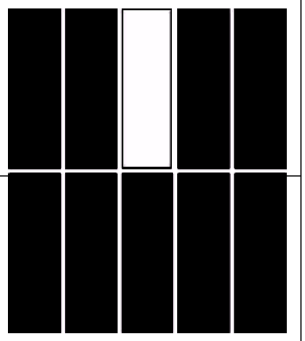
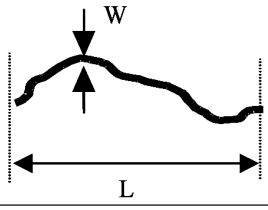
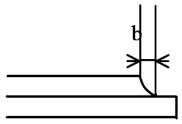
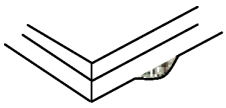
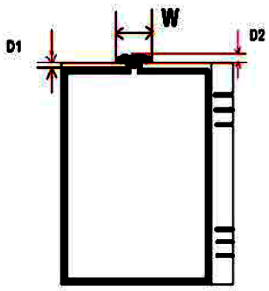
Note 3: Contrast measurements shall be made at viewing angle of $\theta=0^{o}$ and at the center of the LCD surface by using DMS. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See figure 11)

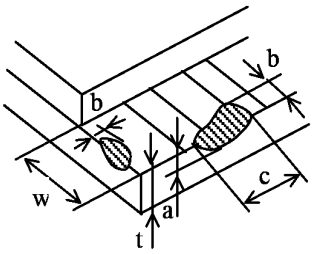
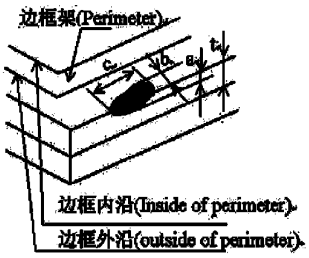
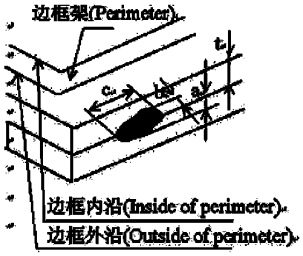
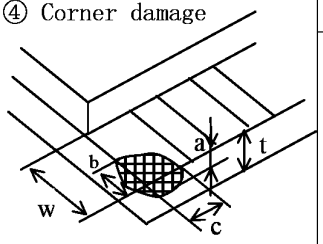
Luminace Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

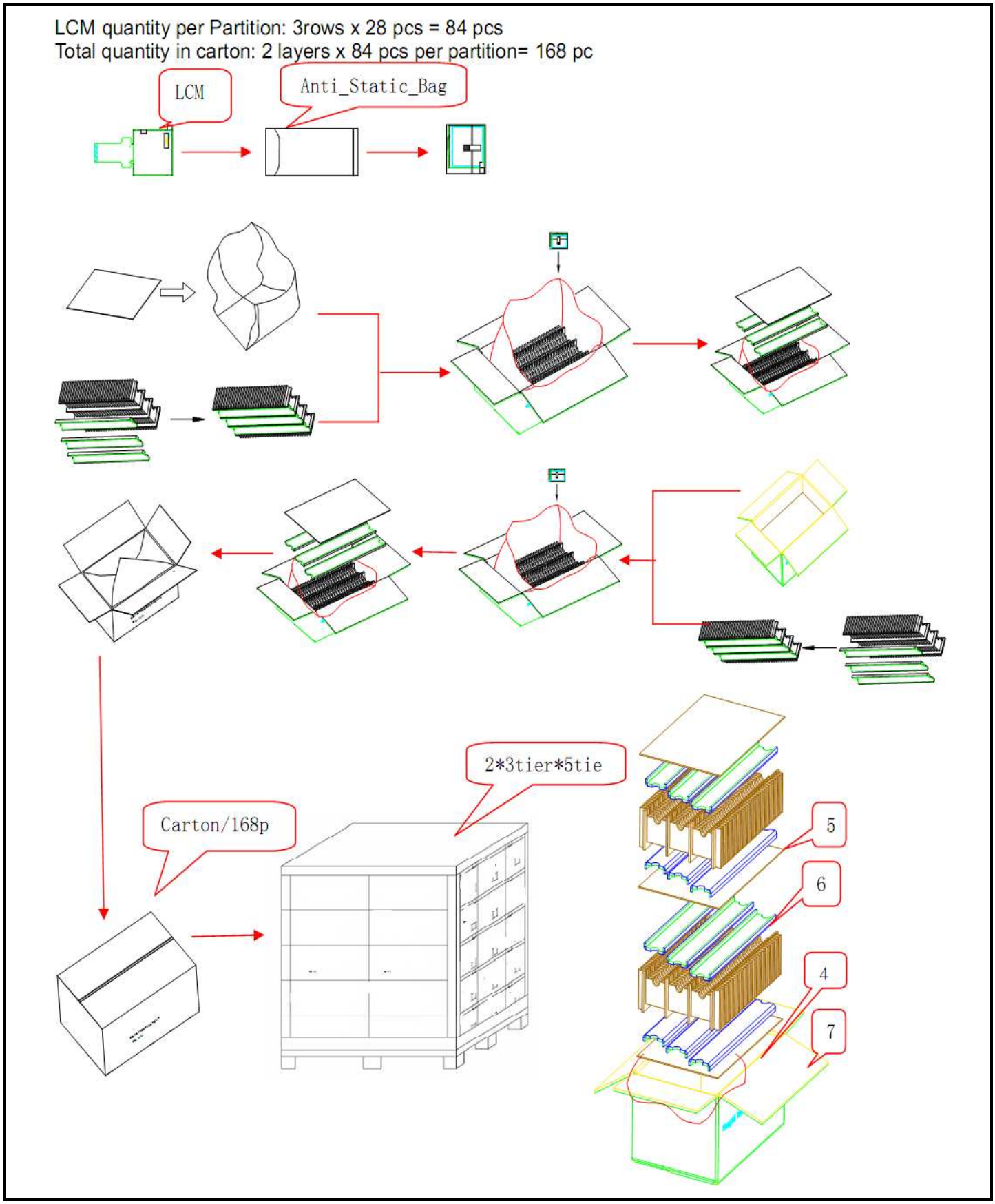
Note 4: The color chromaticity coordinates specified in Table 9 shall be updated from later actual spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

7. TFT Panel Inspection Specifications

Failure mode	Illustration	Category(Unit: mm)		Acceptable count	
				Viewing area	non-Viewing area
Black spot White spot	 Φ= (Length+width)/2	A	Φ≦0.10	Not count	Not count
		B	0.10<Φ≦0.15	2, The gap between the two spots should be 5 mm and above.	
		C	0.15<Φ≦0.20	1	
		D	0.20<Φ	0	
Bright spot(Red spot,green spot and blue spot caused by damaged colour filter)		A	Area≦1 sub-pixel	1	N/A
Black line White line		A	W≦0.03	Not count	Not count
		B	0.03<W≦0.05, L≦3.0	2	
		C	0.05<W	Judged by spot spec	
Below are cosmetic inspection specifications					
Excess glass		b≦1.0, this defect shall not affect the outline dimension or assembly process.(Remarks: For COG process, the defect size is decided by the dimension of LCD panel.)			
		This defect shall not affect the outline dimension or assembly process.			
The depth of UV glue entered in LCD cell		a. D1≥0.2，not enter into viewing area b. D2≦0.8, c. W=End mouth width + (2~6 mm)			

<table>
<tr><td rowspan="5">Glass defect(scratch ,damage)</td><td>① LCD ledge damage
  </td><td colspan="2">Category</td></tr>
<tr><td></td><td>A</td><td>The defect shall not affect the outline dimension or assembly process at non ITO zone.</td></tr>
<tr><td></td><td>B</td><td>b≦1/4w, a & c not count (at ITO zone)</td></tr>
<tr><td></td><td>C</td><td>Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td>② Outside of perimeter damage
  </td><td colspan="2">b can’t reach inside of perimeter.</td></tr>
<tr><td>③ Joint glass damage
  </td><td colspan="2">b can’t reach outside of perimeter or ITO layout.</td></tr>
<tr><td>④ Corner damage
  </td><td>A</td><td>a ≦ t， b ≦ 3.0， c ≦ 3.0</td></tr>
<tr><td colspan="2">B. Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td colspan="4">Remark: a stands for thickness of damage, b for width, c for length and t for glass thickness. (Unit: mm)</td></tr>
</table>

8. Packing demonstrate



9. PRECAUTIONS FOR LCM

Beverly Display Solutions LCMs have been assembled and accurately calibrated before delivery. Please observe the following criteria when handling.

9.1 Static electricity warning

A. Do not take the LCM from its anti-static bag until it's to be assembled.

LCM's are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.

Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. If it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.

The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.

Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screw drivers, are to be first grounded to avoid transmitting spike noises from the motor.

E. Assure that the work bench is properly grounded.

F. Peel off the LCM protective film slowly.

The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could cause static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.

50~60% RH is recommended.

9.2 Precautions for the soldering of a LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.

B. Use a no leakage soldering iron and pay particular attention to the following:

(1) Conditions for soldering I/O terminals

Temperature at iron tip: 280℃ + 10℃

Soldering time: 3~4 sec/terminal

Type of solder: Eutectic solder (rosin flux filled)

Note: (Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning.) Peel off protective film after soldering the I/O terminals. By following this procedure, the surface contamination caused by the dispersion of flux while soldering can be avoided.

(2) Removing the wiring

(When a lead wire, or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole.) If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution: do not reheat the I/O terminal more than 3 times.

9.3 Long-term storage

If the correct method of storage is not followed, deterioration of the display material (polarizer) and oxidation of the I/O terminal plating may make the process of soldering difficult. Please comply with the following procedure.

A. Store in the shipping container.

B. If the shipping container is not available, place in anti-static bags and seal the opening.

C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp.

D. Store in a temperature range of 0℃ - 35℃ with low relative humidity.

9.4 Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40℃ or higher is required, R/H should be less than 60%.

G. Liquid in LCD is hazardous substance. Do not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.